HK829

VOICE RECORDING/PLAYBACK IC 40-60 SEC. PROGRAMMABLE

Features

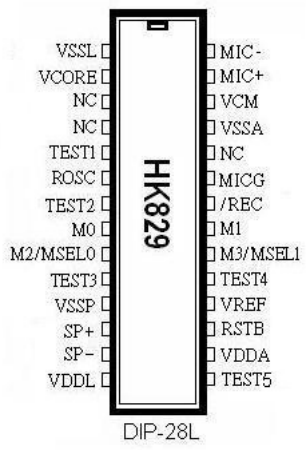
- ◆ Single-chip, high-quality voice recording & playback solution
  - No external ICs required
  - Minimum external components required
- ◆ Non-volatile Flash memory technology
  - No battery backup required
- ◆ User-selectable message record , options by 1,2,4 message
- ◆ Built-in audio-recording microphone amplifier no external amplifier circuits required
- ◆ Configurable analog interface, differential-ended MIC pre-amplifier for low noise with high quality line received
- ◆ DAC and PWM module with high quality analog to digital, resolution up to 16-bits
- ◆ User-friendly, easy-to-use operation
  - Programming & development systems not required
  - Level-activated recording & edge-activated playback switches
- ◆ Low power consumption
  - Standby current: 1μA
  - Automatic power-down, low power down current: 10μA
  - Supports power-down mode for power saving
- ◆ Reset pin for message mode option

General Description

HK829 is powerful audio processor along with high performance audio analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). HK829 is a fully integrated solution offering high performance and unparalleled integration with analog input, digital processing and analog output functionality. It is also quality-enhancing features such as sample-rate convertor

HK829 is specially designed for simple key trigger, user can record and playback the message averagely for 1, 2 or 4 voice message(s) by switch, It is suitable in simple interface or need to limit the length of single message, e.g. toys, leave messages system, answering machine etc. Meanwhile, this mode provides the power-management system. Users can let the chip enter power-down mode when unused. It can effectively reduce electric current consuming to 10uA and increase the using time in any projects powered by batteries.

PinOut Diagram



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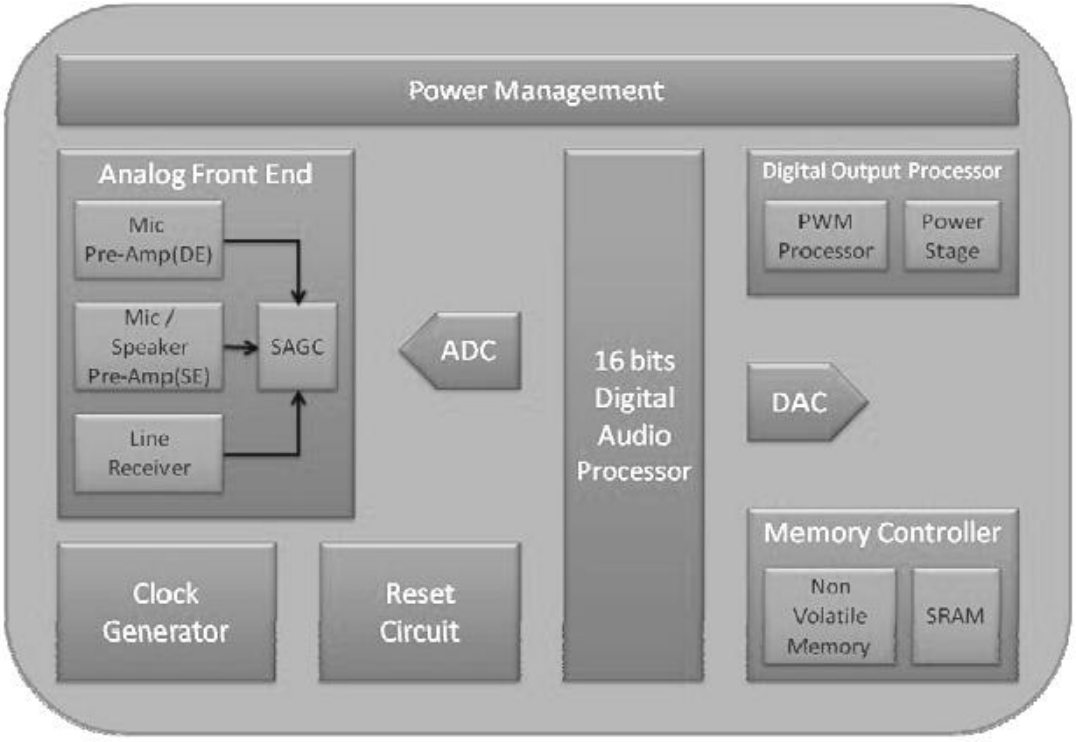
Functional Description

The HK829 block diagram is included in order to give understanding of the HK829's internal architecture. At the left hand side of the diagram are the analog inputs. A differential microphone amplifier, including integrated AGC circuit is included on-chip for applications requiring its use. The amplified microphone signal is fed into the device by connecting the MIC+ , MIC- and MICG pins through an external DC blocking capacitor. Recording can be fed directly into the MIC+ pin through a DC blocking capacitor and resistor, the connection between MIC+, MIC- and MICG are is represented in the lower center of the block diagram. still required for playback. The next block encountered by the input signal is the internal anti-aliasing filter. The filter automatically adjusts its response according to the sampling frequency selected so Shannon's sampling theorem is satisfied. After anti-aliasing filtering is accomplished the storage is accomplished through a combination of the sample and hold circuit and the analog write/read circuit. These circuits are clocked by either the internal oscillator or an external clock source. When playback is desired the previously stored recording is retrieved from memory, low pass filtered, and amplified as shown on the right hand side of the diagram. The signal can be heard by connecting a speaker to the SP+ and SP- pins.
Chip-wide management is accomplished through the device control block shown in the upper right hand corner. Message management signal is ready to be clocked into the memory array. The more detail on actual device application can be found in the sample applications section. More detail on sampling control can be found in the sample rate and voice quality section. More detail on message management and device control' can be found in the message management section.

Block Diagram



Pin Descriptions

Pin name	Pin No.	Type	Description
VDDL	14	Power	Positive power supply
VDDA	16		
VSSL	1	Power	Power ground
VSSP	11		
VSSA	25		
VCORE	2	Power	Positive power supply for core
VREF	18		Reference voltage
VCM	26		Common mode voltage
ROSC	6	Input	Oscillator resistor Input
RSTB	17	Input	Reset (Low active)
MIC+	27	Input	Microphone differential input
MIC-	28		
MICG	23	Output	Microphone ground
SP+	12	Output	Speaker connecting pin for sound output
SP-	13		
/REC	22	Input	Connect to ground for record mode Floating for playback mode
M0	8	Input	Message-0
M1	21	Input	Message-1
M2 / MSEL0	9	Input	Message-2,message select 0
M3 / MSEL1	20	Input	Message-3,message select 1
TEST1	5	X	IC inside test for development engineer use (User no needed to use)
TEST2	7		
TEST3	10		
TEST4	19		
TEST5	15		
N.C.	3 , 4 , 24	X	No connecting

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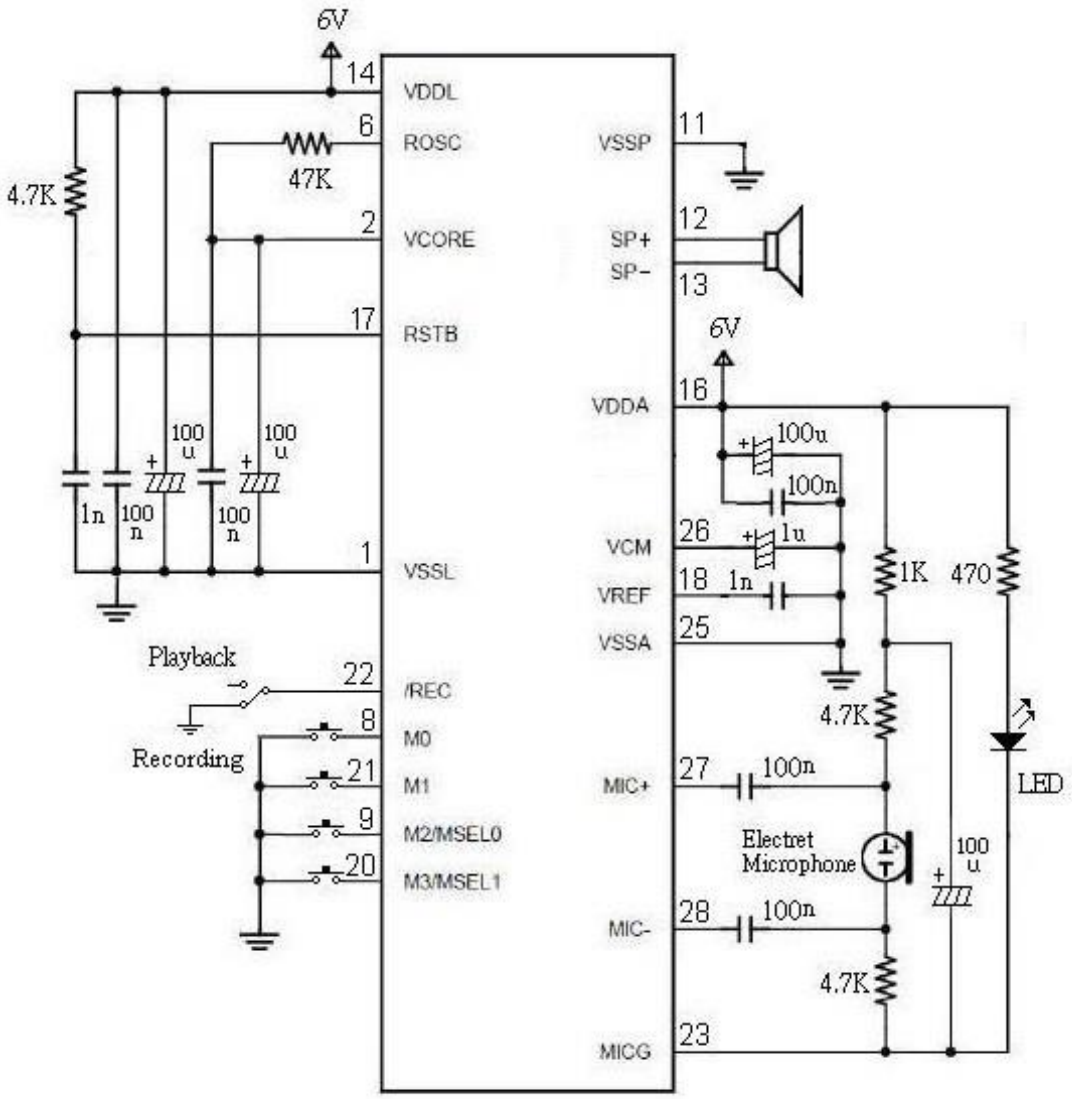
Typical Application Circuit



Function Option

Recording / Playback Message Option

Voice Recording :

During the /REC pin drove to VIL, chip in the recording mode, when the message pin (M0, M1, M2 or M3) drove to VIL in record mode, the chip will playback “beep” tone and message record starting.
The message record will continue until message pin released or full of this message, and the chip will play “beep” tone to indicate the message record finished , if the message already exist and user record again, the old one’s message will be replaced.

Voice Playback:

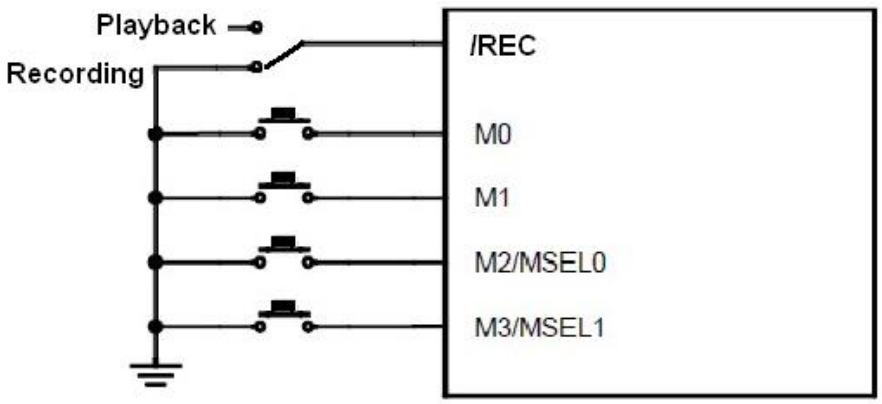
During the /REC pin drove to VIH, chip in the playback mode.
When the message pin (M0, M1, M2 or M3) drove from VIH to VIL in playback mode, the message
The message playback will continue until message pin drove from VIH to VIL again or end of this message
The following fig. showed a typical playback circuit for 4-message mode. We connected a slide-switch between /REC and VSS, and connected 4 tact-switches between M0 ~ M3 and VSS.
When the slide-switch fixed in float side and any tact-switch will be pressed, chip will start message playback and until the user pressed the tact-switch again or end of message.

In fixed 1/ 2/ 4 message mode, user can divide the memory averagely for 1, 2 or 4 message(s).
The message mode will be applied after chip reset by the MSEL0 and MSEL1 pin

Please note :

The message should be recorded and played in same message mode, it **CAN NOT** guarantee that the message is complete after message mode changed. For example, user recorded 4 messages in the 4-message mode, those messages can be played in 4-message mode only. If user changed to 1 or 2 message mode, system will discard those messages.

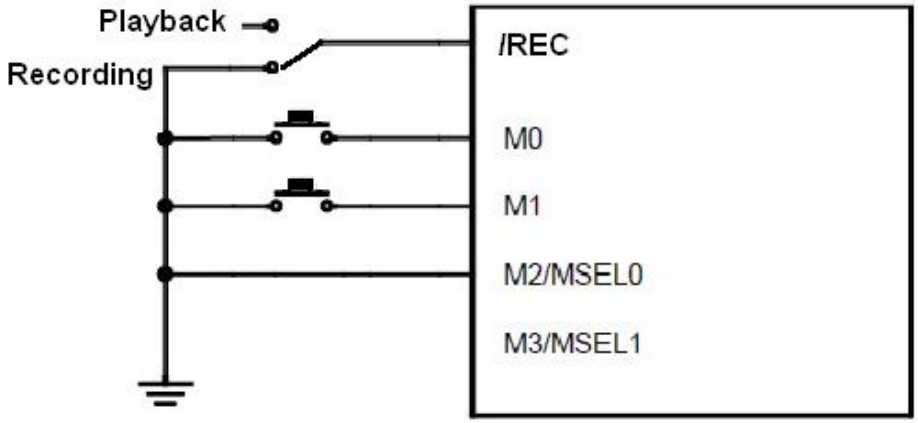
4 Messages Mode :



The memory will be divided to 4 messages averagely when both MSEL0 and MSEL1 pin float after chip reset

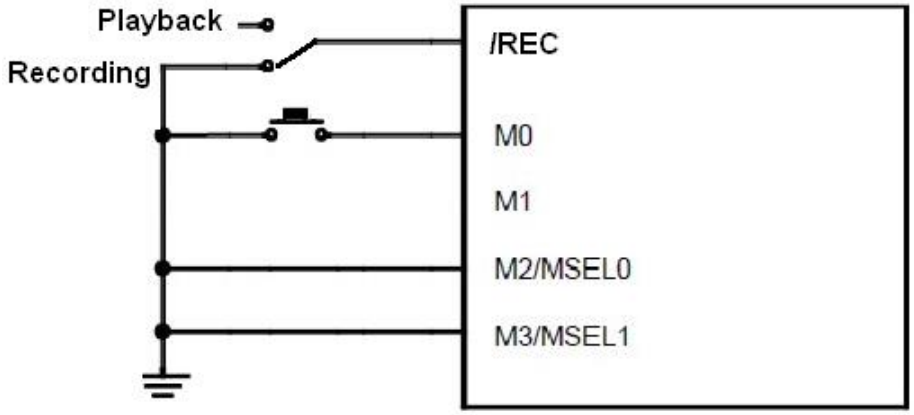
2 Messages Mode :

The memory will be divided to 2 messages averagely when M2/MSEL0 pin connected to VSS and M3/MSEL1 pin float after chip reset



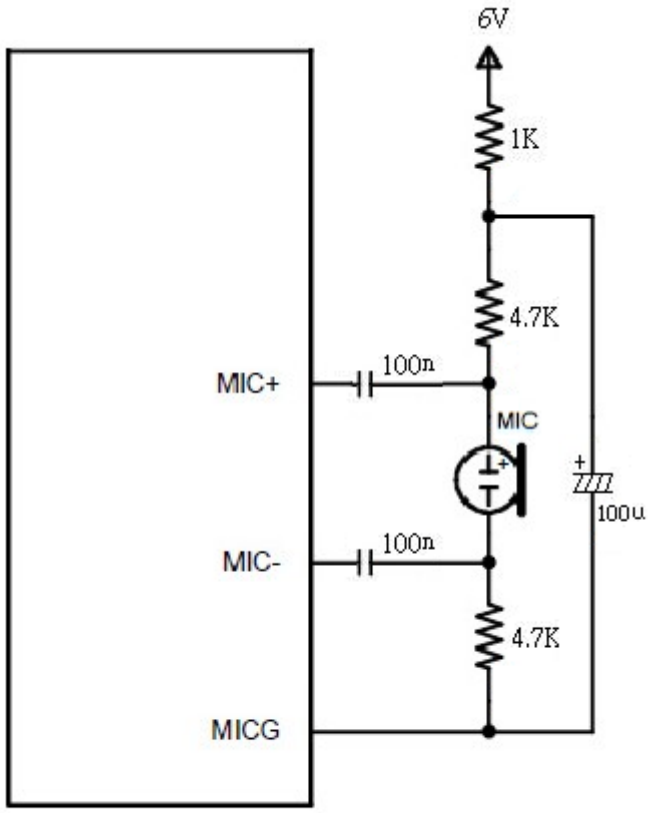
1 Messages Mode :

The memory will be for 1 message when both MSEL0 and MSEL1 pin connected to VSS after chip reset



Voice Input

The HK829 supported single channel voice input by microphone or line-in. The following fig showed circuit for different input methods: microphone, line-in and mixture of both.



Voice input from microphone

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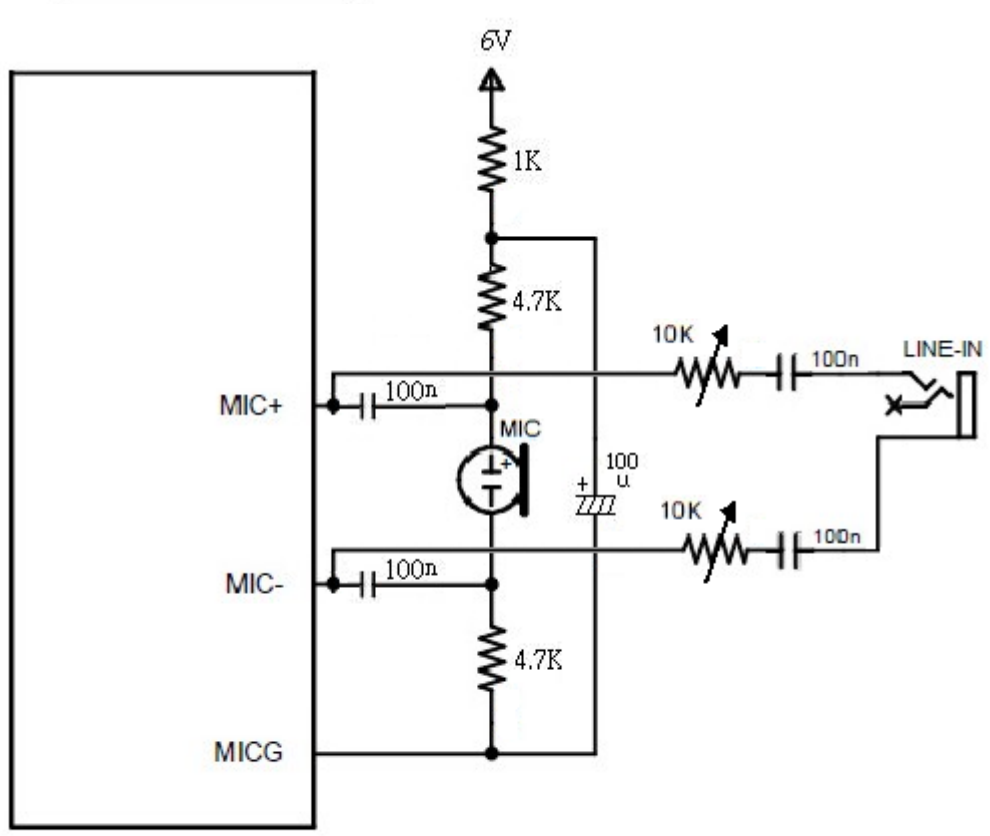
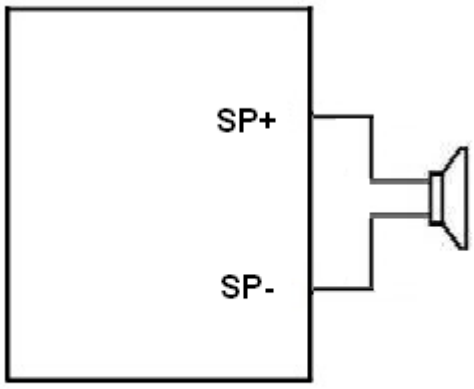


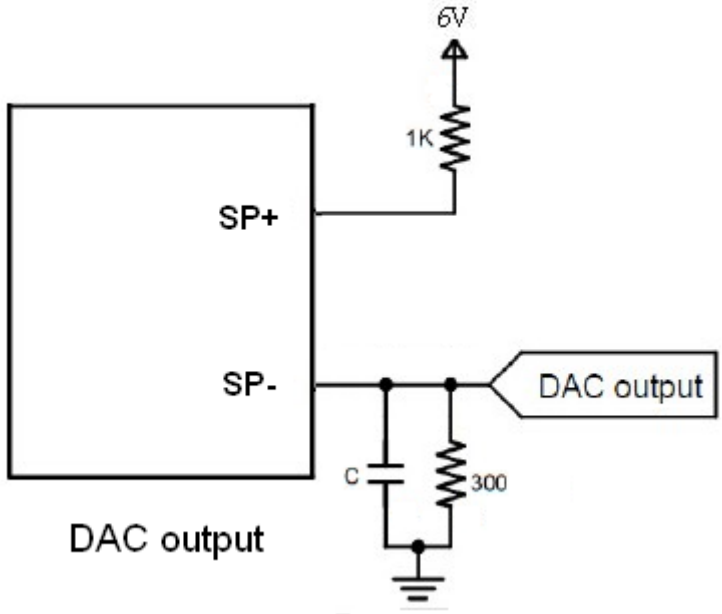
Voice input from microphone & line in both

Voice Output

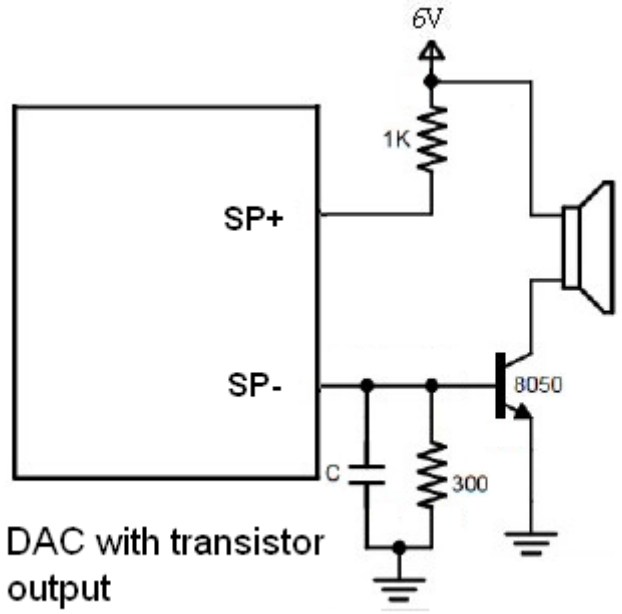
The HK829 support 2 voice output mode, PWM and DAC
PWM mode : To use SP+ and SP- pin to drive a speaker directly without external components to save cost
DAC mode : SP- pin to output current signal, user can use the signal to external audio amplifier, or mix, with other components in their applications to provide larger voice volume



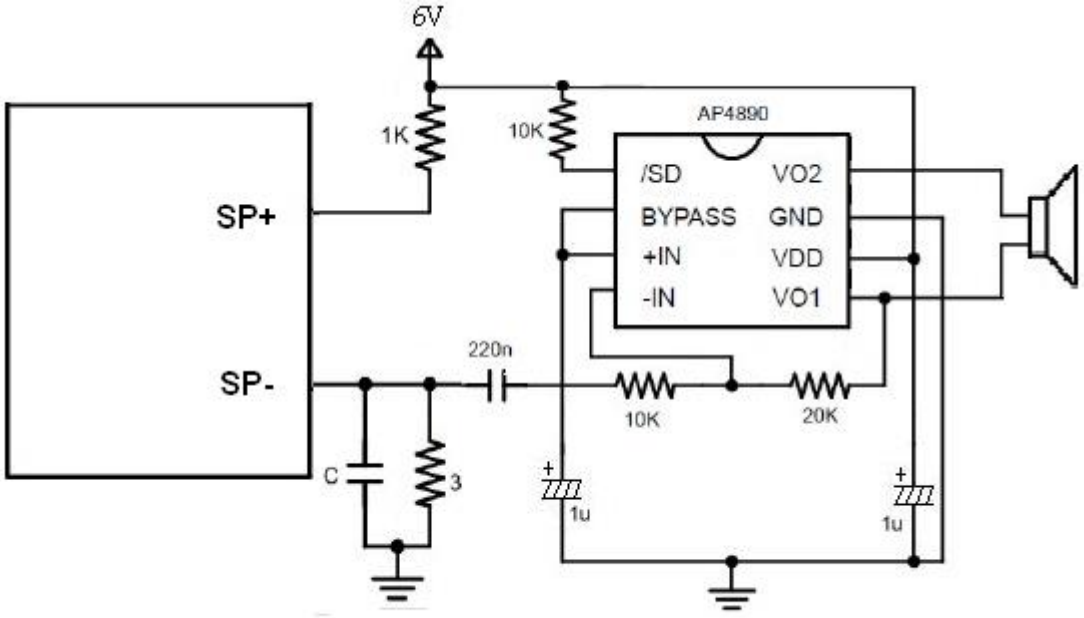
PWM output



DAC output



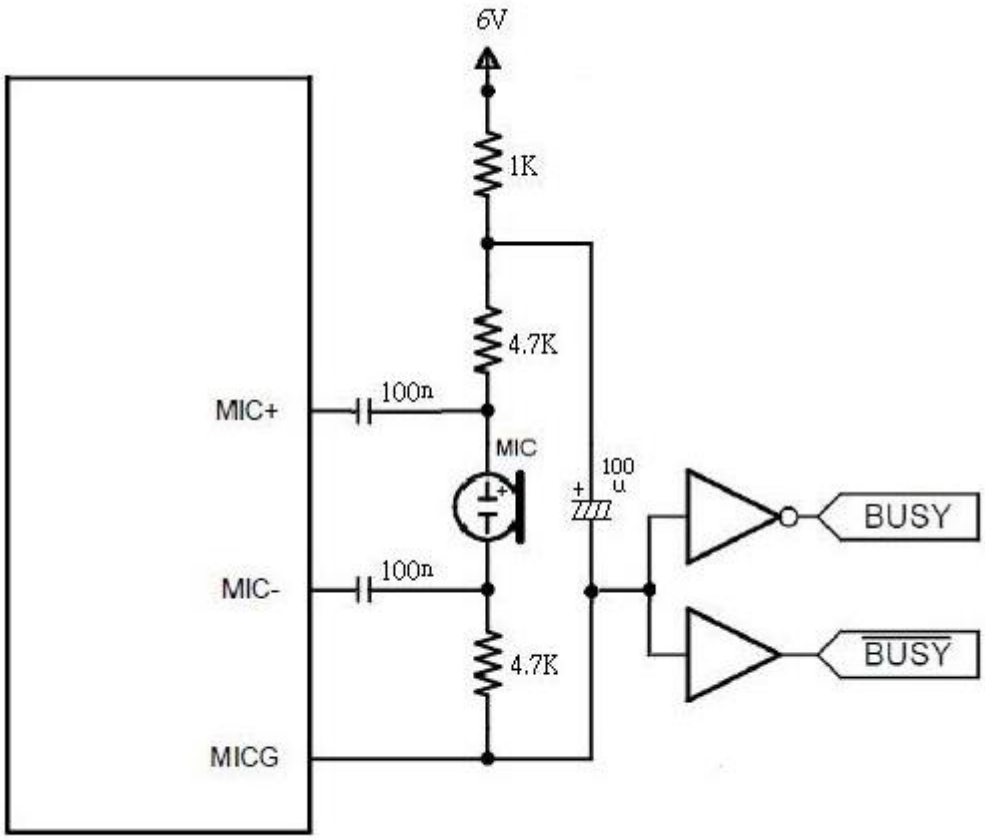
DAC with transistor output



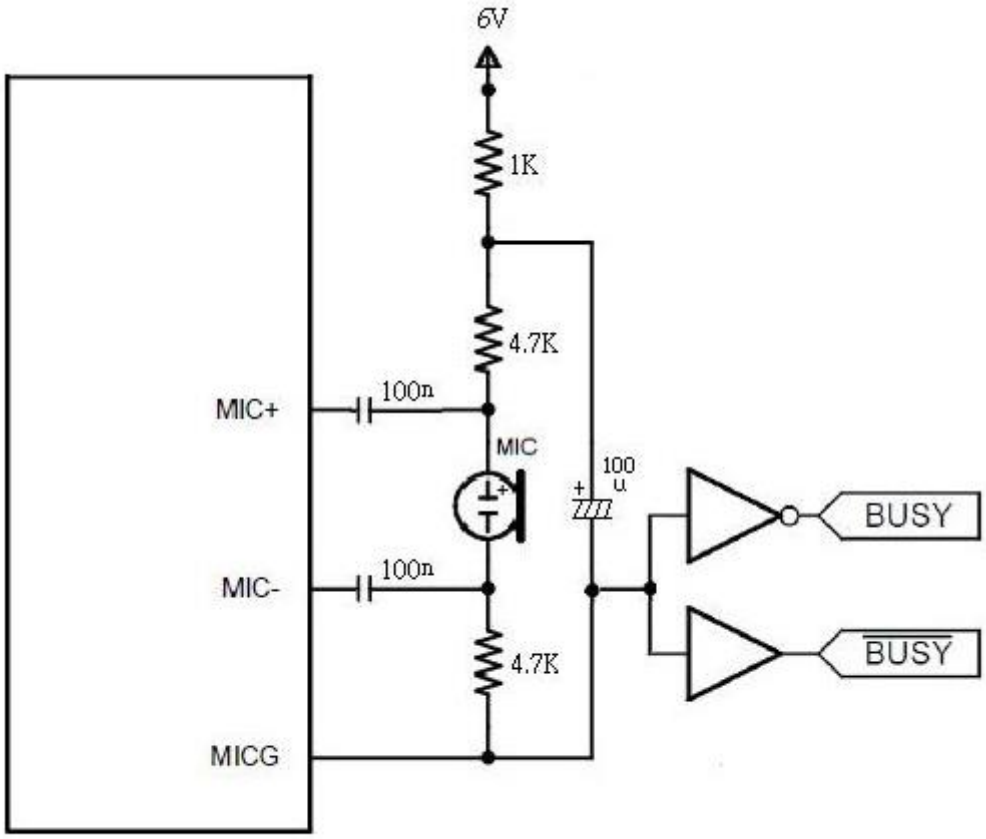
DAC with AP4890 IC Amp. output

BUSY Signal

The MICG pin will be drove to low during the message record or playback, and drove to high during idle or standby, user can detect MICG status to know chip is busy or not.



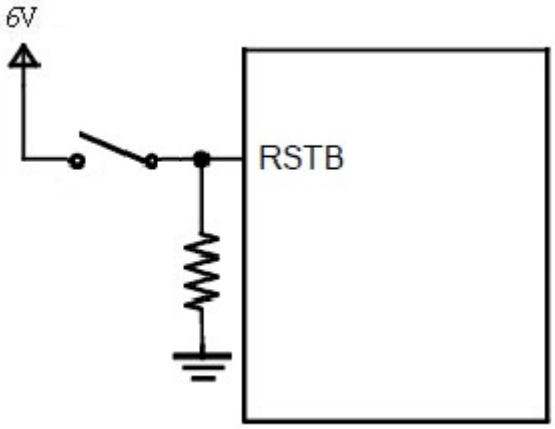
Buffer & inverter for BUSY signal



Buffer & inverter for BUSY signal

RESET Signal

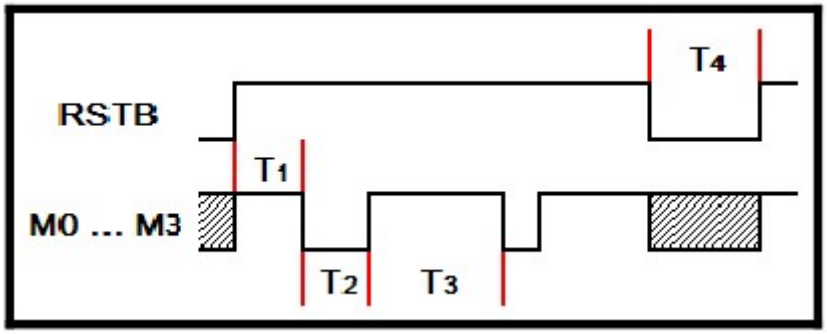
The HK829 can enter standby mode when RSTB pin drive to low. During chip in the standby mode, the current consumption is reduced to ISB and any operation will be stopped, user also can not execute any new operate in this mode. The standby mode will continue until RSTB pin goes to high, chip will be started to initial, and playback “beep” tone to indicate enter idle mode. User can get less current consumption by control RSTB pin specially in some application which concern standby current



Sample Rate Table

Recording Duration	ROSC Resistor Value	Sample Rate
42 Seconds	47 KΩ	12 KHz
46 Seconds	63 KΩ	11 KHz
51 Seconds	79 KΩ	10 KHz
56 Seconds	100 KΩ	9 KHz
64 Seconds	120 KΩ	8 KHz
73 Seconds	143 KΩ	7 KHz
85 Seconds	173 KΩ	6 KHz

RTS (Reset) and M0 , M1 , M2/MSEL0 , M3/MSEL1 Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T1	System Initial Time	100			mS	VDD=5.0V
T2	Trigger Setup Time	16			mS	VDD=5.0V
T3	Trigger Hold Time	16			mS	VDD=5.0V
T4	Reset Hold Time	100			μS	VDD=5.0V

Electrical Characteristics

The following tables list Absolute Maximum Ratings, DC Characteristics, and Analog Characteristics for the HK829 device.

Absolute Maximum Ratings

Item	Sym.	Condition	Min	Typ.	Max	Unit
Power Supply voltage	V_{cc}	T_A = 25℃	3.8	6.0	6.9	V
Input Voltage	V_{IN2}	I_{IN}<20mA	-1.0	-	V_{CC} + 1.0	V
Storage Temperature	T_{STG}	-	-65	25	150	℃
Temperature Under Blas	T_{BS}	-	-65	25	125	℃
Lead Temperature	T_{LD}	<10s	-0.3	25	300	℃

DC Characteristics

Item	Sym.	Condition	Min	Typ.	Max	Unit
Power Supply voltage	V_{CC}	T_A = 25℃	4.5	6	6.9	V
Input High Voltage	V_{IN}	-	2.0	-	-	V
Input Low Voltage	V_{IL}	-	-	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -1.6 mA	2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = - 4.0 mA	-	-	0.45	V
Output Tristate Leakage Current	I_{OZ}	V_{OUT} = V_{CC} or V_{OUT} = V_{SS}	-1.0	-	1.0	μA
Operating Current Consumption	I_{CC}	Internal Clock, No Load	-	25	-	mA
Standby Current Consumption	I_{CCS}	No Load	-	1.0	-	μA

Analog Characteristics*

Item	Sym.	Condition	Min	Typ.	Max	Unit
Micin Input Voltage	V_{MI}	-	-	-	30	$_{m}V_{p-p}$
Micin Input Resistance	R_{MI}	-	-	15	-	kΩ
Micin Amp Gain (1)	G_{MI1}	AGC = 2.25v	-	30	-	dB
Micin Amp Gain (2)	G_{MI2}	AGC = 3.8V	-	-2	-	dB
Anain Input Voltage	V_{ANI}	-	-	-	140	$_{m}V_{p-p}$
Anain Input Resistnce	R_{ANI}	-	-	500	-	kΩ
Anain Amp Gain	G_{ANI}	AnaIn to SP +/-	-	10	-	dB
AGC Output Resistance	R_{AGC}	-	-	225	-	kΩ
Sp +/- Output Power	P_{SP}	$R_{SP\ +/-}$ = 16Ω	-	12.2	-	mW
Voltage Amplitude across SP+/-	V_{SP}	$R_{SP\ +/-}$ ≧ 16Ω	-	1.4	-	V_{p-p}

Package Outlines

The HK829 device is available in the DIP package form , Packages conform to JEDEC and EIAJ standards.

28-Pin Plastic Dual In-Line Package (DIP-28L, P-600)